First Hit

☐ Generate Collection Print

L3: Entry 6 of 174 File: PGPB Apr 4, 2002

DOCUMENT-IDENTIFIER: US 20020039436 A1
TITLE: Optical inspection apparatus for defect detection

Abstract Paragraph:
A method and apparatus for inspecting the surface of articles, such as chips and wafers, for defects, includes a first phase of optically examining the complete surface of the article inspected at a relatively high speed and with a relatively low spatial resolution, and a second phase of optically examining with a relatively high spatial resolution only the suspected locations for the presence or absence of a defect therein.

Application Filing Date:
20010119

Summary of Invention Paragraph:
[0008] According to the present invention, there is provided a method of inspecting the surface of articles for defects, comprising: placing the article to be inspected on a table; in a first phase, optically examining the complete surface of the article on the table at a relatively high speed and with a relatively low spatial resolution; electrically outputting information indicating suspected locations on the article having a high probability of a defect; storing the outputted information in a storage device; and in a second phase, while the article is still on the table, optically examining with a relatively high spatial resolution only the suspected locations stored in the storage device for the presence or absence of a defect in the suspected locations.

Summary of Invention Paragraph:
[0009] According to further features of the invention, the first examining phase is effected by optically scanning the complete article surface to be inspected; and the second examining phase is automatically effected immediately after the first phase by imaging only the suspected locations on a converter which converts the images to electrical signals and then analyzes the electrical signals.

Summary of Invention Paragraph:
[0010] According to still further features in preferred embodiments of the invention described below, the surface of the article to be inspected includes a pattern, e.g., a patterned wafer used for producing a plurality of integrated-circuit dies or chips. The first examining phase is effected by making a comparison between the inspected pattern and another pattern, serving as a reference pattern, to identify locations on the inspected pattern wherein there are sufficient differences with respect to the reference pattern to indicate a high probability of a defect in the inspected pattern. The second examining phase is also effected by making a comparison between the inspected pattern and the reference pattern, to identify locations on the inspected pattern wherein the comparison shows sufficient differences with respect to the reference pattern to indicate the presence of a defect in the suspected location of the inspected pattern.

Summary of Invention Paragraph:
[0012] It will thus be seen that the novel method of the present invention primarily monitors changes in the defect density while maintaining a high

throughput with a relatively low false alarm rate. Thus, the first examination is done at a relatively high speed and with a relatively low spatial resolution to indicate only suspected locations having a high probability of a defect; and the second examination is done with a relatively high spatial resolution but only with respect to the suspected locations having a high probability of a defect. The sensitivity of the two phases may be adjusted according to the requirements for any particular application. Thus, where the application involves a relatively low number of defects, the sensitivity of the first examination phase may be increased to detect very small defects at a high speed but at the expense of an increased false alarm rate. However, since only relatively few suspected locations are examined in the second phase, the overall inspection can be effected relatively quickly to enable the fabrication personnel to identify defects caused by any process or equipment, and to immediately correct the cause for such defects.

Summary of Invention Paragraph:
[0013] According to a further feature of the invention, the first examining phase is effected by generating a first flow of N streams of data representing the pixels of different images of the inspected pattern unit; generating a second flow of N streams of data representing the pixels of different images of the reference pattern unit; and comparing the data of the first flow with the data of the second flow to provide an indication of the suspected locations of the inspected pattern unit having a high probability of a defect.

Summary of Invention Paragraph:
[0016] According to still further features of the invention, the second examining phase is effected by imaging on a converter each suspected location of the inspected pattern unit and the corresponding location of the reference pattern unit to output two sets of electrical signals corresponding to the pixels of the inspected pattern unit and the reference pattern unit, respectively; and comparing the pixels of the inspected pattern unit with the corresponding pixels of the reference pattern unit to indicate a defect whenever a mismatch of a predetermined magnitude is found to exist at the respective location. Each suspected location of the inspected pattern unit and the reference pattern unit is imaged at a plurality of different depths, and the electric signals of one set are shifted with respect to those of the other set to match the respective depths of the images.

Brief Description of Drawings Paragraph:
[0023] FIG. 4 is a diagram illustrating the optic system in the first examining phase of the apparatus of FIG. 1;

Brief Description of Drawings Paragraph:
[0028] FIGS. 9-11 are diagrams illustrating the manner of scanning the wafer in the Phase I examination;

Brief Description of Drawings Paragraph:
[0029] FIG. 12 is a block diagram illustrating the Phase I processing system;

Brief Description of Drawings Paragraph:
[0041] FIG. 26 is a diagram illustrating the main elements of the Phase II optic system;

Brief Description of Drawings Paragraph:
[0042] FIGS. 27-31 are diagrams illustrating the construction and operation of the Phase II examination system;

Brief Description of Drawings Paragraph:
[0045] FIG. 36 is an optical diagram corresponding to FIG. 26, but illustrating modifications in the Phase II examination;

Brief Description of Drawings Paragraph:

[0046] FIG. 37 is a diagram helpful in explaining the modifications in the Phase II examination;

Brief Description of Drawings Paragraph:
[0047] FIGS. 38 and 39 are block diagrams corresponding to FIGS. 27 and 28, respectively, but showing the changes in the Phase II examination;

Detail Description Paragraph:
[0056] The system illustrated in the drawings is designed particularly for automatically inspecting patterned semiconductor wafers having a plurality of like integrated-circuit dies each formed with like patterns. The system inspects each pattern, called the inspected pattern, by comparing it with at least one other pattern on the wafer, serving as the reference pattern, to detect any differences which would indicate a defect in the inspected pattern.

Detail Description Paragraph:
[0057] The inspection is made in two phases: In the first phase, the complete surface of the wafer is inspected at a relatively high speed and with a relatively low spatial resolution; and information is outputted indicating suspected locations on the wafer having a high probability of a defect. These locations are stored in a storage device. In the second phase, only the suspected locations stored in the storage device are examined with a relatively high spatial resolution; and a determination is made as to the presence or absence of a defect. This facilitates identification and correction of the process that created the defect.

Detail Description Paragraph:
[0058] The inspection apparatus illustrated in FIGS. 1-3 of the drawings includes a table 2 for receiving the wafer W to be inspected. The first phase inspection of the wafer is by a laser 3 outputting a laser beam which scans the complete surface of the wafer W; and a plurality of light collectors 4 arranged in a circular array to collect the light scattered from the wafer and to transmit the scattered light to a plurality of detectors 5. The outputs of the detectors 5 are fed via a Phase I preprocessor 6 to a Phase I image processor 7, which processes the information under the control of a main controller 8. The Phase I image processor 7 processes the outputs of the detectors 5 and produces information indicating suspected locations on the wafer having a high probability of a defect. These suspected locations are stored within a storage device in the main controller 8.

Detail Description Paragraph:
[0059] Only the suspected locations having a high probability of a defect are examined by the Phase II examining system. This system includes an optic system for imaging the suspected location on an opto-electric converter, e.g., a CCD matrix 9, which converts the images to electric signals. These signals are fed via a Phase II preprocessor 10 to a Phase II image processor 11 which, under the control the main controller 8, outputs information indicating the presence or absence of a defect in each suspected location examined in Phase II.

Detail Description Paragraph:
[0060] In the block diagram illustrated in FIG. 2, the table 2 of FIG. 1, and associated elements involved in the wafer handling system, are indicated generally by block 12, Table 2 is controlled by a movement control system, indicated by block 13, to effect the proper positioning of the wafer on the table 2 in each of the Phase I and Phase II examination phases, and also the scanning of the wafer W in the Phase I examination.

Detail Description Paragraph:
[0061] The light detectors 5 of FIG. 1 are included in the Phase I image acquisition sensor indicated by block S.sub.1 in FIG. 2; and the opto-electric converter 9 of FIG. 1 is included within the Phase II image acquisition sensor indicated by block S.sub.2 in FIG. 2.

Detail Description Paragraph:
[0062] FIG. 2 also illustrates a post processor 14 processing the information from the Phase I processor 7; the main controller 8 which manages and synchronizes the data and controls the flow; a keyboard 15 enabling the operator to input information into the main controller 8; and a monitor 16 enabling the operator to monitor the processing of the information.

Detail Description Paragraph:
[0063] All the elements in the wafer handling and image acquisition subsystem for both phases are included within the broken-line box generally designated A in FIG. 2; all the elements of the image processor subsystem (both the algorithms and the hardware) for both phases are indicated by the broken-line block B; and all the elements in the operator console subsystem are indicated by the broken-line block C. The latter subsystem includes not only the main controller 8, keyboard 15, and monitor 16, but also a graphic terminal unit, shown at 17 in FIG. 1.

Detail Description Paragraph:
[0068] The subsection illustrated in FIG. 3 also includes the movement controller 13 controlled by the main controller 8. Movement controller 13 controls a one-directional scanning stage 21. This stage moves a vacuum chuck 24 which holds the wafer flattened during its movement in one orthogonal direction with respect to the Phase I sensors 5, as the laser beam from the laser 3 is deflected in the other orthogonal direction to scan the complete surface of the wafer during the Phase I examination.

Detail Description Paragraph:
[0069] Movement controller 13 further controls a two-dimensional scanning stage 22 effective, during the Phase II examination, to position the wafer at any desired position with respect to the Phase II detector 9 (the CCD matrix). As described in detail below, the control of one of the axes of this stage serves also during the Phase I examination. Movement controller 13 further controls a rotation/level/focus stage 23, which rotates the wafer about its axis to align it angularly, to level it, and to keep it in focus during scanning. Stage 23 also roves the vacuum chuck 24 and its wafer towards or away from the Phase II sensor 9 to enable producing a plurality of images at different depths during the Phase II examination, as will be described more particularly below.

Detail Description Paragraph:
[0072] Phase I Optic System

Detail Description Paragraph:
[0073] As shown in FIG. 4, the laser 3 (e g., an argon laser) outputs a laser beam which is passed through a polarizer beam splitter 30 oriented in such a way to transmit the laser light to the wafer W, but to reflect the reflected light from the wafer to a photodetector 31. The latter outputs an electric signal controlling the Phase I preprocessor 6. The laser beam from beam splitter 30 is passed through a beam expander 32, then through a cylindrical lens 33a, a deflector 34, another cylindrical lens 33b, a folding mirror 35, a multi-magnification telescope 36, a beam splitter 37, a quarter wavelength plate 38 which converts the linearly polarized light to a circularly polarized light and vice versa, and finally through a microscope objective 39, which focuses the laser beam on the wafer W.

Detail Description Paragraph:
[0082] As shown in FIG. 9, the wafer W being inspected is formed with a plurality of integrated-circuit dies D.sub.1-D.sub.n each including the same pattern. In the Phase I examination, the complete surface of the wafer is scanned by the laser beam 3, and the resulting scattered light is collected by the above-described light collectors 42 in order to detect defects, or at least those suspected areas having a high likelihood of including a defect and therefore to be more carefully examined

during the Phase II examination. As also indicated above, during the Phase I examination (and also the Phase II examination), the pattern of one die D, serving as the inspected pattern, is compared with the light pattern of at least one other die, serving as the reference pattern, to determine the likelihood of a defect being present in the inspected pattern.

Detail Description Paragraph:
[0083] FIGS. 9-11 illustrate the manner of carrying out the scanning of the wafer in the Phase I examination.

Detail Description Paragraph:
[0089] As indicated earlier, the Phase I examination system may include eight light detectors 46 (or four light detectors where the variation of FIGS. 6a-8a is used) for inspecting the wafer for defects. However, it may also include a further detector (a reflected light detector) to provide additional information for the registration procedure. Thus, the misalignment may be detected from the reflected light detector image by computing the cross-correlation between a rectangle of pixels in the inspected image, and the rectangle of pixels in the reference image in all possible misalignments. This information may be used where the score matrix computed in the alignment control circuit does not provide a significant indication of the correct misalignment.

Detail Description Paragraph:
[0090] Phase I Image Processor

Detail Description Paragraph:
[0091] The Phase I examination is effected by: (a) generating a first flow of N streams of data (N being the number of light collectors 42, or 42') representing the pixels of different images of the inspected pattern; (b) generating a second flow of N streams of data representing the pixels of different images of the reference pattern; and (c) comparing the data of the first flow with the data of the second flow to provide an indication by the comparison of the suspected locations of the inspected pattern having a high probability of a defect. The comparison is effected by correcting any misalignment between the two flows of data; comparing the data of each stream of the first flow with the data of the corresponding stream of the second flow to provide a difference or alarm value indicating the significance of the presence of a suspected pixel in the stream; and detecting a defect at a pixel location according to N difference or alarm values corresponding to the N streams of data.

Detail Description Paragraph:
[0092] FIG. 12 is a functional block diagram of the Phase I image processor. It includes an input from each of the eight sensors 46a-46b (each corresponding to photodetector sensor 46 in FIG. 7) to their respective preprocessors 6a-6g. The sensors convert the light signals to analog electrical signals, and the preprocessors sample the latter signals at pixel intervals and convert them to digital data. The outputs of the preprocessors are thus in the form of streams of pixel values forming a digital version of the image.

Detail Description Paragraph:
[0099] The post processor 14 receives the list of suspected defects, together with their relevant parameters, and makes decisions before passing them on to the main controller for processing by the Phase II image processor system. It outputs a list of suspected points to transmit to the Phase II examination system, including their parameters, and also a list of defects which will not be transmitted to the Phase II examination system.

Detail Description Paragraph:
[0110] The Score Calculator 73 computes the score matrix of correlation between the inspected and reference images in all the possible shifts around the current pixel,

up to the maximum allowed. It receives three inputs: (a) the inspected image, to define the area around which the correlation is checked; (b) the reference image, to define the range of possible matches within the maximum range of horizontal and vertical shifts; and (c) a control input, from Pixel Characterizer 72, allowing the choice of registration points on the basis of pixel type.

Detail Description Paragraph:
[0121] For every registration point the correspondence of its 3.times.3 pixels neighbourhood is measured against pixels in a range of .+-.A in the corresponding stream. FIG. 14a illustrates the algorithm. For each of the (2R.rarw.1).times. (2R.rarw.1) possible misalignments, a correlation measure is computed as the normalized sum of absolute difference. The correlation matrices computed for different registration points are summed, and the minimal value in the matrix corresponds to the correct misalignment.

Detail Description Paragraph:
[0122] The Score Calculator 73, as described earlier with reference to FIG. 14, computes the score matrix of correlation between the inspected and reference images in all the possible shifts around the current pixel, up to the maximum allowed plus or minus vertical and horizontal ranges). This unit includes the following circuits: delays 73a, 73b, to correct the timing of the arrival of the inspected and reference images, respectively, to that of the arrival of the Registration Point flags from the pixel characterizer 72; Neighbourhood Normalizers 73c, 73d, to normalize the pixels in the neighbourhood of the current pixel; Absolute Difference Calculator 73e, which finds the absolute difference between the inspected image in the vicinity of the current pixel as against all the possible matches in the reference image within the maximum range of shifts in the vertical and horizontal axes, and computes the score matrix for these matches; and Score Matrix accumulator 73f which sums and stores all the score matrices which are accumulated during the scanning of a number of successive rows, before transmitting them to the Alignment Computer 62 (FIG. 12) for computation of the best match.

Detail Description Paragraph:
[0144] 4. Gradient--indicates if the pixel is located in a slope area of 3.times.3 pixels relative to a threshold defined dynamically in a window of n.times.m pixels. 5 g (F 2 , 2) = 1 if max F 0 i T 6 i = 1 , 2 i = 1 , 2

Detail Description Paragraph:
[0178] The result of the normalized difference between the inspected image and the reference image is outputted every clock pulse, until all possible combinations of the 3.times.3 adjacent pixels within the search window are completed.

Detail Description Paragraph:
[0181] The Registration Score Matrix Calculator 73j illustrated in FIG. 22 is more particularly shown in FIG. 23. It computes the score matrix based on the normalized difference between the inspected image (3.times.3 pixels in extent), and all the N.times.N possible matches in the corresponding matrix in the reference image.

Detail Description Paragraph:
[0182] Calculator 73j includes a Pixel Normalizer 81 (FIG. 23) for the inspected image; a Pixel Normalizer 82 for the reference image; a Difference Calculator 83; a Summation Calculator 84; a Division Table 85; a Multiplier 86; a Results Storage device 87; and a Score Accumulator 88.

Detail Description Paragraph:
[0188] Difference Calculator 83 computes the sum of the absolute differences of the 3.times.3 matrix of the inspected image versus the reference image. For this purpose, Calculator 83 includes, for each of the two Pixel Normalizers 81 and 82. a Subtraction Circuit 83a, 83b consisting of nine subtractors which compute the difference between each pixel in the inspected image versus the corresponding pixel

in the reference image; an Absolute Value Circuit 83c, 83d, which computes the absolute value of the differences; and a Matrix Circuit 83e, 83f, which sums all the nine absolute values. The result of the absolute sum of the differences is passed to the Multiplier 86.

Detail Description Paragraph:
[0191] Multiplier 86 computes the result o the normalized difference for the point under test. The computation is carried out using the formula:

Detail Description Paragraph:
[0196] Each of the nine comparisons is made by comparing the difference between the energies of the compared pixels against a threshold determined by the pixel type. The energy of a pixel is the sum of the nine pixels in the 3.times.3 neighbourhood centered at the pixel. The alarm value is set to "2", if the difference in all nine comparisons is above the high threshold; to "1", if it is above the low threshold; and to "0" in all other cases.

Detail Description Paragraph:
[0203] The post-processor 14 (FIG. 12) thus receives the list of suspected defects, together with their relevant parameters, and makes decisions before passing them onto the Phase II examination system. These decisions include: (a) clustering; (b) choosing the points which will be passed to Phase II; and (c) the optimum route in Phase II. The latter functions are carried out by microprocessor programs.

Detail Description Paragraph:
Phase II Examination

Detail Description Paragraph:
[0205] As briefly described earlier, the Phase II examination is effected automatically upon the completion of the Phase I examination while the wafer is still on the table 2, but only with respect to those locations of the wafer W indicated during the Phase I examination as having a high probability of a defect. Thus, while the Phase I examination is effected at a relatively high speed and with a relatively low spatial resolution, the Phase II examination is effected at a much lower speed and with a much higher spatial resolution, to indicate whether there is indeed a defect in those locations suspected of having a defect during the Phase I examination.

Detail Description Paragraph:
[0206] Briefly, the Phase II examination is effected by: imaging on converter 9 (FIGS. 1 and 26), e.g., a CCD, each suspected location of the inspected pattern, and the corresponding location of the reference pattern, to output two sets of electrical signals corresponding to the pixels of the inspected pattern and the reference pattern, respectively; and comparing the pixels of the inspected pattern with the corresponding pixels of the reference pattern to indicate a defect whenever a mismatch of a predetermined magnitude is found to exist at the respective location. To accommododate variations in the thickness of the wafer and/or pattern, and/or multi-layer patterns each suspected location of the inspected pattern, and the reference pattern is imaged at a plurality of different depths, and the electric signals of one set are shifted with respect to those of the other set to match the respective depths of the images.

Detail Description Paragraph:
[0207] Phase II Optic System

Detail Description Paragraph:
[0208] The Phase II optic system is shown generally in FIG. 1 and more particularly in FIG. 26. It includes a microscope objective 100 mounted in a rotating turret 101 carrying different objectives to enable bringing a selected one into the optical path between the wafer W and the image converter 9. The wafer W is illuminated by a

flashlamp unit 102 via an optical device 103 having a beamsplitter 104 and a second beamsplitter 105. Unit 102 also contains a continuous light source, such as a standard tungsten lamp, which is used with a standard TV camera 110 and/or viewing system III, described below.

Detail Description Paragraph:
[0210] Phase 2 Image Processor

Detail Description Paragraph:
[0211] FIG. 27 illustrates both the Phase 2 image preprocessor 10 and the Phase 2 image processor 11.

Detail Description Paragraph:
[0213] FIG. 27 further illustrates the Phase 2 image processor 11 as including a hardware accelerator 129 for accelerating particularly the registration and comparison operations.

Detail Description Paragraph:
[0215] As described earlier, the input to the Phase II image processor includes two sets of images, taken from the inspected pattern and the reference pattern, respectively. Each set includes five images taken with focusses at different depths in order to accommodate variations in the thickness of the wafer or pattern, or to accommodate multi-layer patterns.

Detail Description Paragraph:
[0218] FIGS. 29-31 more particularly illustrate how the depth matching operation is performed. Thus, the sequence of images taken from the inspected pattern is matched with those taken from the reference pattern. The goal is to match each image of the inspected pattern with the image of the reference pattern taken at the corresponding depth of focus. Two assumptions are made: (1) the images are taken in the order of increasing depth with a fixed difference between each two consecutive images; and (2) the error in the depth of the first image of the two sequences is at most the difference between two consecutive images.

Detail Description Paragraph:
[0219] Hence. if I.sub.i, 1.ltoreq.i.ltoreq.5 and R.sub.i, 1.ltoreq.i.ltoreq.5 are the inspected and reference images, respectively, the matching procedure detects x, where x is one of -1,0 or 1 such that (I.sub.i,R.sub.i+x) is a pair of comparable images (see FIG. 29), for i=1, . . . , 5. Correlation in the depth of focus of two images to measured by computing similarity in the variance of grey levels in the two images. The correlation measure used is the difference between the grey level histograms of the images. The shift x is computed as the one providing the best correlation for all images in the sequence.

Detail Description Paragraph:
[0222] (2) Compute the distance between the histograms (block 133). The distance is taken as the sum of absolute differences between corresponding cells in the histograms. The distance will be computed as follows:

Detail Description Paragraph:
[0229] As described above, both the Phase I and the Phase II examinations may be effected by a die-to-die comparison or by a repetitive-pattern comparison of repetitive pattern units on the same die (or other article). FIG. 32 illustrates such a repetitive pattern on the same die.

Detail Description Paragraph:
[0230] The repetitive pattern illustrated in FIG. 32 consists of a number of relatively small (e.g. a few microns in size) comparable units. A typical comparable unit in a repetitive-pattern comparison is shown as the area bounded by the dashed line 200 in FIG. 32. As therein shown, each pixel along the scanning

line 202 is comparable to a pixel which is located at a distance "d" either to its left or to its right. Since the two pixels that have to be compared are contained in the same scanning line, no registration has to be done between the "inspected" and the "reference" image, as will be shown below.

Detail Description Paragraph:
[0231] FIGS. 33, 34 and 35 are block diagrams which correspond to FIGS. 12, 14 and 24, respectively (which figures relate to a die-to-die comparison in the Phase I examination), but show the changes involved in a repetitive-pattern comparison. To facilitate understanding, and also to simplify the description, only those changes involved in the repetitive-pattern comparison of FIGS. 33, 34 and 35 are described herein; in addition, comparable elements are generally correspondingly numbered as in FIGS. 12, 14 and 24, respectively, except are increased by "200".

Detail Description Paragraph:
[0232] With respect to the overall functional block diagram illustrated in FIG. 33, the system receives as inputs: (1) signals from the N sensors (N-8 in the illustrated embodiment), and (2) a shift control signal 204 which determines the distance (in pixels) between the current pixel and the shifted pixel to which the current pixel is compared. The shift (in pixels) corresponds to the distance "d" in FIG. 32, and is supplied to the system by the user prior to an inspection operation. The system processes the N input signals and outputs a list of locations suspected as defects.

Detail Description Paragraph:
[0238] FIG. 34 illustrates one channel in the processing system of FIG. 33 for a repetitive-pattern comparison. It will be seen that the following units appearing in the corresponding FIG. 14 (for a die-to-die comparison) are absent in FIG. 34 (1) the pixel characterizer 72; (2) the score matrix calculator 73; (3) the reference die memory 15; and (4) the pixel aligner 76. The first two of the above units (72, 73) deal with the registration between the reference and the inspected die; and since registration is not needed in a repetitive-pattern comparison, they are omitted from FIG. 34. The reference die memory 75; and the pixel aligner 76 are replaced by the cycle shifter 276a. As mentioned earlier, the shift control signal 204 determines the amount of shift (in pixels) between the reference pixels and types (inputs a and b to the comparator 272), and the corresponding inspected pixels and types (inputs c and d to the comparator 272).

Detail Description Paragraph:
[0239] FIG. 35 illustrates more particularly the Defect Detector Portion of the image processor of FIG. 34, and corresponds to FIG. 24. This circuit compares each pixel to its corresponding shifted pixel according to the shift amount determined by the shift control signal 204; and the comparison generates a one-channel alarm for each pixel having a signal which is significantly larger than their corresponding shifted pixels.

Detail Description Paragraph:
[0240] Following are the main differences between the circuit illustrated in FIG. 35 (for a repetitive-pattern comparison) with respect to the system of FIG. 24 (for a die-to-die comparison): The reference die memory (75, FIG. 24) and the pixel aligner (76, FIG. 24) are replaced by the cycle shifter 276a, as described above. The cycle shifter 276a generates a shift (in pixels) which corresponds to the comparable unit distance (d) in FIG. 34. The shifter amount is determined by the shift control input 204. The cycle shifter 276a has three inputs: (a) inspected pixels, (b) inspected types, and (c) shift control signal 204. The cycle shifter 276a is a standard shift register with programmable length. The delay length is determined by the shift control signal 204.

Detail Description Paragraph:
[0241] Improvements in Phase II Examination

Detail Description Paragraph:
[0242] FIGS. 36-39 illustrate a number of improvements in the Phase II examination system described above. FIG. 36 generally corresponds to FIG. 26, but illustrates certain modifications to be described below; FIG. 37 is a diagram helpful in explaining these improvements; and FIGS. 38 and 39 generally correspond to FIGS. 27 and 28, but show the modifications also to be described below. To facilitate understanding and to simplify the description, only the changes included in FIGS. 36, 38 and 39, as compared to FIGS. 26, 27 and 28 are specifically described below; in addition generally comparable elements are identified by the same reference numerals except increased by "300", and now elements are identified by reference numerals starting with "400".

Detail Description Paragraph:
[0243] A main difference in the optical system illustrated in FIG. 36, as compared to FIG. 26, is that the FIG. 36 optical system uses darkfield imaging of the object, rather than brightfield imaging. Thus, it has been found that darkfield imaging increases the sensitivity to small defects, compared to standard brightfield imaging. Using darkfield imaging in the Phase II examination is superior in confirming or rejecting alarms detected in Phase I, thereby producing a higher probability of detection and a smaller probability of false alarms.

Detail Description Paragraph:
[0244] The Phase II optical system as shown in FIG. 36 includes a darkfield microscope objective 300 mounted in a rotating turret 301 carrying different objectives to enable bringing a selected one into the optical path between the wafer W and the image converter 309. The wafer W is illuminated by an illumination unit 400 via an optical device 303 including beam splitters 304 and 305. Unit 400 is a standard unit. based on a mercury lamp, such as supplied by Leitz. It consists of a 200 watt mercury lamp 402, a reflector 404, and a condenser 406.

Detail Description Paragraph:
[0249] The imaging of the locations identified as having a high probability of a defect as a result of the Phase I examination, is accomplished as follows: the wafer is first moved by means of the XY stage (22, FIG. 3) so that the possible defect detected by the Phase I examination is located beneath the Phase II objective 300 (FIG. 36). The autofocus 306 focusses the lens at a predetermined depth relative to the object's surface by moving the rotation/level/focus stage 323 to the proper Z-position.

Detail Description Paragraph:
[0253] FIG. 38 illustrates both the Phase II image preprocessor 310 and the Phase II image processor 311.

Detail Description Paragraph:
[0255] FIG. 38 further illustrates the Phase II image processor 311 as including a hardware accelerator 329 for accelerating particularly the comparison operation.

Detail Description Paragraph:
[0257] The input to the Phase II image processor includes a set of images taken from the inspected pattern in the neighbourhood of a suspected location designated by the Phase I image processor. A set includes five images taken with focusses at different depths in order to accommodate variations in the thickness of the wafer or pattern, or to accommodate multi-layer patterns.

Detail Description Paragraph:
[0260] Circuit 327 compares the gray level images, pixel by pixel, using surrounding pixels and adaptive thresholds obtained from a threshold computation circuit 329. The latter circuit computes the thresholds at each pixel location according to the feature detector contained in circuit 324.

Detail Description Paragraph:
[0309] In the preferred embodiments of the invention described above, both the Phase I examination and the Phase II examination are effected, one automatically after the other. It is contemplated. however, that the invention, or features thereof, could also be embodied in apparatus which effects only the first examination or only the second examination. It is also contemplated that the apparatus could be supplied with the capability of effecting both examinations but with means for disabling, e.g., the second examination, if not required for any particular application. Many other variations, modifications and applications of the invention will be apparent.

CLAIMS:

1. A method of inspecting the surface of articles for defects, comprising: placing the article to be inspected on a table; in a first phase, optically examining the complete surface of the article on the table inspected at a relatively high speed and with a relatively low spatial resolution; electrically outputting information indicating suspected locations on the article having a high probability of a defect; storing said outputted information in a storage device; and in a second phase, while the article is still on said table, optically examining with a relatively high spatial resolution only said suspected locations stored in said storage device for the presence or absence of a defect in said suspected locations.

2. The method according to claim 1, wherein said first examining phase is effected by optically scanning the complete article surface to be inspected; and said second examining phase is automatically effected immediately after the first phase by imaging only said suspected locations on a converter which converts the images to electrical signals and then analyzes said electrical signals.

3. The method according to claim 1, wherein said surface of the article includes a pattern to be inspected; and said first examining phase is effected by making a comparison between the inspected pattern and another pattern serving as a reference pattern, and identifying locations on the inspected pattern wherein the comparison shows sufficient differences with respect to the reference pattern to indicate a high probability of a defect in the inspected pattern.

4. The method according to claim 3, wherein said second examining phase is also effected by making a comparison between the inspected pattern and the reference pattern, and identifying locations on the inspected pattern wherein the comparison shows sufficient differences with respect to the reference pattern to indicate the presence of a defect at the suspected location of the reference pattern.

8. The method according to claim 5, wherein said first examining phase is effected by the following operations: generating a first flow of N streams of data representing the pixels of different images of the inspected pattern unit; generating a second flow of N streams of data representing the pixels of different images of the reference pattern unit; and comparing the data of said first flow with the data of the second flow to provide an indication of the suspected locations of the inspected pattern unit having a high probability of a defect.

9. The method according to claim 8, wherein said comparing operation is effected by: correcting any misaligmnent between the two flows of data; comparing the data of each stream of the first flow with the data of the corresponding stream of the second flow to provide an alarm value indicating the significance of the presence of a suspected location in the stream; and detecting a defect at a pixel location according to N alarm values corresponding to the N streams of data.

10. The method according to claim 5, wherein said first examining phase is effected

by a laser beam which is deflected to scan a line along one orthogonal axis, while the article to be inspected is physically displaced along a second orthogonal axis.

11. The method according to claim 5, wherein said second examining phase is effected by the following operations: imaging on a converter each suspected location of the inspected pattern unit and the corresponding location of the reference pattern unit is output two sets of electric signals corresponding to the pixels of the inspected pattern unit and the reference pattern unit, respectively; and comparing the pixels of the inspected pattern unit with the corresponding pixels of the reference pattern unit to indicate a defect whenever a mismatch of a predetermined magnitude is found to exist at the respective location.

18. The method according to claim 17, wherein said comparing operation is effected by: correcting any misalignment between the two flows of data; comparing the data of each stream of the first flow with the data of the corresponding stream of the second flow to provide an alarm value indicating the significance of the presence of a suspected location in the stream; and detecting a defect at a pixel location according to N alarm values corresponding to the N streams of data.

21. The method according to claim 18, wherein said comparing operation includes: assigning a type to each pixel in each of the N streams of each flow; comparing each pixel in each stream of one flow with the corresponding pixel in the corresponding stream of the other flow with respect to predetermined thresholds which depend on the type assigned to the respective pixel; and assigning an alarm value to the pair of pixels in each comparison in each stream indicating the probability of a defect in the location of the inspected pattern unit corresponding to the respective pixels.

22. The method according to claim 18, wherein said comparison is further effected by detecting a defect at a pixel location according to the combination of the N alarm values corresponding to the N streams of data.

24. The method according to claim 23, wherein said predetermined parameters include: (a) local maxima, indicating whether the pixel is a maximum relative to its noighbours; (b) intensity, indicating whether the intensity of the pixel is significant relative to a predetermined threshold; (c) ratio of intensity, indicating whether the intensity of the pixel is significant with respect to its neighbours relative to its predetermined threshold; and (d) gradient, indicating whether the pixel is located in a sloped area with neighbouring pixels relative to a predetermined threshold.

41. Inspection apparatus for inspecting the surface of articles for defects, comprising: a table for receiving the article to be inspected; first examining means overlying said table for examining in a first phase the complete surface of the article thereon at a relatively high speed and with a relatively low spatial resolution, and for outputting information indicating suspected locations on the article surface having a high probability of a defect; storage means for storing the output of said first examining means; and second examining means overlying said table for examining, in a second phase and with a relatively high spatial resolution, only said suspected locations stored in said storage means, and for outputting information indicating the presence or absence of a defect in the suspected location.

44. The apparatus according to claim 41, wherein: the article to be examined has a plurality of comparable pattern units to be inspected, by comparing each such unit. identifying as an inspected pattern unit, with at least one other pattern unit, identified as a reference pattern unit; and said first examining means includes means for outputting information identifying locations on the inspected pattern unit in which the comparison shows sufficient differences with respect to the

reference pattern unit to indicate a high probability of defect in the inspected pattern unit.

48. The apparatus according to claim 47, wherein said processor includes: misalignment correcting means for correcting any misalignment between the two flows of data: comparison means for comparing the date of each stream of the first flow with the data of the corresponding stream of the second flow to provide an alarm value indicating the significance of the presence of a suspected pixel in the stream; and detector means for detecting a defect at a pixel location according to N alarm which are corresponding to the N streams of data.

56. The apparatus according to claim 55, wherein said processor includes: misalignment correcting means for correcting any misalignment between the two flows of data; comparison means for comparing the data of each stream of the first flow with the data of the corresponding stream of the second flow to provide an alarm value indicating the significance of the presence of a suspected pixel in the stream; and detector means for detecting a defect at a pixel location according to N alarm values corresponding to the N streams of data.

61. The apparatus according to claim 60, wherein said comparison means includes means for detecting a defect at a pixel location according to the combination of the N alarm values corresponding to the N streams of data.

62. The apparatus according to claim 61, wherein said assigning means assigns each pixel one of a plurality of types according to the following parameters: (a) local maxima, indicating whether the pixel is a maximum relative to its neighbours; (b) intensity, indicating whether the intensity of the pixel is significant relative to a predetermined threshold; (c) ratio of intensity, indicating whether the intensity of the pixel is significant with respect to its neighbours relative to its predetermined threshold; and (d) gradient, indicating whether the pixel is located in a sloped area with neighbouring pixels relative to a predetermined threshold.

88. The method according to claim 5, wherein said repetitive pattern units are spaced from each other a predetermined distance such as to define repetitive pattern zones, and the suspected locations outputted from said first phase are restricted to locations in said repetitive pattern zones.

89. The apparatus according to claim 45, wherein said like patterns in all said dies are spaced from each other a predetermined distance such as to define repetitive pattern zones; and said first examining means includes means for suppressing from the suspected locations outputted from said first phase those locations not in said repetitive pattern zones.